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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,065	02/20/2004	Takeshi Shimizu	073338.0177 (04-50094 FLA	6302

5073 7590 02/15/2008

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EXAMINER	
JONES, PRENELL P	

ART UNIT	PAPER NUMBER
2619	

NOTIFICATION DATE	DELIVERY MODE
02/15/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/783,065	SHIMIZU ET AL.	
	Examiner	Art Unit	
	Prenell P. Jones	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that neither the reference of Bellenger (US Pat 5,949,786) or Simmons (US Pat 6,084,856) fail to teach a plurality of memory banks logically divided into a plurality of rows, wherein each of the rows include a storage location from each of the memory banks, and an overflow buffer that includes a plurality of overflow storage locations.

After reviewing cited prior art, Examiner has decided to withdraw previous rejection, however, an additional search was performed, and additional prior art has been found.

Claim Rejections - 35 USC § 103

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bellenger (US Pat 5,949,786) in view of Runaldue et al (US Pat. 6,175,902).

Regarding claim 1, 3, and 8, Bellenger discloses a communication a multi-protocol switch that manages and monitoring accessible locations for storing routing information, wherein the architecture includes multiple ports, tagging storage locations (Fig. 2, Abstract, col. 2, line 41-67, col. 4, line 47-56), a switch fabric for receiving packets between ports (Fig. 2, col. 4), and a memory control module for receiving an memory access request from ports, and determining rows based on address indicated by the request (Figs. 2-5, col, 5).

However, Bellenger is silent on memory logically divided into a plurality of rows, wherein each row includes storage location for memory, and overflow buffer having multiple storage location and maintaining routing entry and to access row and the overflow buffer to perform a memory access operation.

In a switch communication system, Runaldue et al (US Pat. 6,175,902) discloses maintaining memory associated in a switching environment, wherein memory is logically divided into rows and columns (Abstract, col. 2, line 51-67), and multiple overflow queues (overflow areas/overflow buffers 110, 120, 122, 124, 128 and so on), and each row associated with memory buffer includes n locations for storage (col. 9, line 54-63, col. 11, line 13-53).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to memory logically divided into a plurality of rows, wherein each row includes storage location for memory, and overflow buffer having multiple storage location and maintaining routing entry and to access row and the overflow buffer to perform a memory access operation as taught by Runaldue with the teachings of Bellenger for the purpose of further managing the storing of data flow in a switch environment whereas to minimize cost and increase efficiency.

Regarding 2, Bellenger further discloses address memory access requesting lookup operation (Fig. 2), and receiving routing entries from rows (col. 4, line 47 thru col. 5, line 61), each entry in route table contains tag (potential routing entries), accessed entries is used to determine a match (Fig. 3 & 6, col. 5, line 5-60)

Although, Bellenger is silent on overflow buffer and comparing address against each of the entries.

Runaldue further discloses in a switch utilizing overflow management and monitoring with respect with overflow area, wherein matching frame pointer address are searched with respect to the number of entries (col. 18, line 6-13)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement overflow buffer including a matching entry, and utilizing overflow management and monitoring with respect with overflow area, wherein matching frame pointer address are searched with respect to the number of entries, as taught by Runaldue with the teachings of Bellenger for the purpose of further managing the storing of data flow in a switch environment whereas to minimize cost and increase efficiency.

Regarding claim 4, Bellenger further discloses an arbitration module to receive lookup/learn request (Fig. 2), and memory access module for a series of memory access operations (series of hash codes) to determine a hash key from an address indicates a specific row (col. 4, line 57-67, col. 6, line 34-60) generates and processes as associated with ports and generating hash keys wherein a row associated with a flow buffer is indicated by a hash key (col. 4, line 47-67).

Regarding claim 5, Bellenger further discloses an arbitration module that schedules memory access operations with respect to lookup and learn request (Fig. 5, col. 6, line 21-60, col. 8, line 23-36, col. 9, line 7-46).

Regarding claim 6, Bellenger further an arbitration module servicing a learn request (Fig. 2, Fig. 5, col. 6, line 21-60, col. 8, line 23-36, col. 9, line 7-46) and determining whether a read operation detected a miss in a memory bank, whereas a write operation indicates a source to port map from learn request (Fig. 4, Abstract, col. 5, line 5-61).

Regarding claim 7, 12, 16 and 20, Bellenger further discloses flow detect filters, which stores data in registers, wherein the filters are used to select or de-select processing operations, such as write operation with respect to accessing memory (Abstract, col. 3, line 33-56).

Regarding claim 9, Bellenger further discloses storage elements associated with a plurality of ports and associated rows and flow buffers/overflow buffer for processing memory access (col. 4, line 23 thru col. 5, line 16, col. 6, line 21-34).

Regarding claim 10 and 15, as indicated above, combined Bellenger and Runaldue discloses a communication a multi-protocol switch that manages and monitoring accessible locations for storing routing information, wherein the architecture includes multiple ports, tagging storage locations (Fig. 2, Abstract, col. 2, line 41-67, col. 4, line 47-56), a switch fabric for receiving packets between ports (Fig. 2, col. 4), and a memory control module for receiving an memory access request from ports, and determining rows based on address indicated by the request (Figs. 2-5, col, 5), and discloses maintaining memory associated in a switching

environment, wherein memory is logically divided into rows and columns (Abstract, col. 2, line 51-67), and multiple overflow queues (overflow areas/overflow buffers 110, 120, 122, 124, 128 and so on), and each row associated with memory buffer includes n locations for storage (col. 9, line 54-63, col. 11, line 13-53).

Bellenger further discloses generating hash from flow, and determining hash key based on destination address, wherein matching of hash key and hash codes with respect to table for the addressed entries (Fig. 2, 5 & 6, col. 8, line 23-55)

Although, Bellenger is silent on overflow buffer including a matching entry, returning routing information from the matching entry, the routing information identifying at least one port,

Runaldue further discloses in a switch environment, matching entries as associated with address and forwarding routing information to identified port (col. 18, line 6-13, col. 22, line 30-67)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement overflow buffer including a matching entry, returning routing information from the matching entry, the routing information identifying at least one port, a switch utilizing overflow management and monitoring with respect with overflow regions, as taught by Runaldue with the teachings of Bellenger for the purpose of further managing the storing of data flow in a switch environment whereas to minimize cost and increase efficiency.

Claim 18 includes the limitations of method claim 10, but in the form of a physical switch. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement a switching architecture that is constructed to further implement the functions of claim 10.

Regarding claim 11 and 19, Bellenger further discloses learn/look-up processing wherein a routing table is associated with selected hash values and hash coding, wherein hash values are generated based on incoming address, and wherein the hash is utilized in conjunction with address and rows (Fig. 6, col. 3, line 33-55, col.4, line 50-67).

Regarding claims 13 and 14, Bellenger further discloses decision steps on matching address entries with respect to source and destination addresses (Figs. 3 & 4, col. 5, line 5-62), wherein rows of data are compared with "matching entries, as well as, determining addressable locations (available storage location) for storage (col. 2, line 51 thru col. 3, line 31, col. 4, line 47-67).

Claims 21 and 22 include the limitations encompassed in claims 13 and 14, but in the form of a switching device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement a switching architecture that is constructed to further implement the functions of claim 10.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prenell P. Jones whose telephone number is 571-272-3180. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Wing Chan can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prenell P. Jones PJ

December 31, 20007

1/4/08

WING CHAN
SUPERVISORY PATENT EXAMINER